TRANSMITTAL OF APPEAL BRIEF

Docket No.
SON-3173

In re Application of: Masaaki Bairo

Application No.	Filing Date	Examiner	Group Art Unit
10/584,994-Conf. #5930	June 29, 2006	W. W. Kuo	2826

Invention: BIPOLAR TRANSISTOR, SEMICONDUCTOR APPARATUS HAVING THE BIPOLAR TRANSISTOR, AND METHODS FOR MANUFACTURING THEM

TO THE COMMISSIONER OF PATENTS:

Transmitted herewith is the Appeal Brief in this application, with respect to the Notice of Appeal filed: May 22, 2008 .

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40,290

Dated: September 9, 2008

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Docket No.: SON-3173
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Masaaki Bairo

Application No.: 10/584,994 | Confirmation No.: 5930

Filed: June 29, 2006 | Art Unit: 2826

For: BIPOLAR TRANSISTOR, SEMICONDUCTOR APPARATUS HAVING THE BIPOLAR TRANSISTOR, AND METHODS FOR MANUFACTURING THEM | Examiner: W. W. Kuo

APPELLANT'S BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is an Appeal Brief under 37 C.F.R. §41.37 appealing the final decision of the Examiner dated February 22, 2008. Each of the topics required by 37 C.F.R. §41.37 is presented herewith and is labeled appropriately. This brief is in furtherance of the Final Office Action on February 22, 2008.

A Notice of Appeal was filed in this case on May 22, 2008, along with a Request for Panel Review. The Notice of Panel Decision from Pre-Appeal Brief Review mailed on August 18, 2008. ("the Decision") indicates that claims 9-15 remain rejected. The Decision further indicates that the extendable time period for the filing of the Appellant's Brief will be reset to be one month from the mailing of the Decision, or the balance of the two-month time period running from the receipt of the notice of appeal, whichever is greater.

Accordingly, the filing of the Appellant's Brief is timely. 37 C.F.R. §1.136.

I. REAL PARTY IN INTEREST

Sony Corporation of Tokyo, Japan ("Sony") is the real party in interest of the present application. An assignment of all rights in the present application to Sony was executed by the inventor and recorded by the U.S. Patent and Trademark Office at **Reel 018035, Frame 0384.**

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Within the Final Office Action of February 22, 2008:

Paragraph 4 of the Office Action indicates a rejection of claims 9-13 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 6,307,227 (Fujii) in view of U.S. Patent No. 5,013,677 (Hozumi), and further in view of U.S. Patent No. 6,885,081 (Morimoto).

Paragraph 11 of the Office Action indicates a rejection of claims 14-15 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 6,307,227 (Fujii) in view of U.S. Patent No. 5,013,677 (Hozumi), and further in view of U.S. Patent No. 6,885,081 (Morimoto), and further in view of U.S. Patent Application Publication No. 2003/0235984 (Besser).

Thus, the status of the claims is as follows:

Claims 1-8: (Canceled);

Claims 9-15: (Rejected).

No claims are indicated within the Final Office Action to contain allowable subject matter.

Accordingly, Appellant hereby appeals the final rejection of claims 9-15 which are presented in the Claims Appendix.

IV. STATUS OF AMENDMENTS

Provided is a statement of the status of any amendment filed subsequent to final rejection.

Subsequent to the final rejection of February 22, 2008, an Amendment After Final Action Under 37 C.F.R. 1.116 has been filed on March 13, 2008.

The Advisory Action dated March 27, 2008 indicates that the Amendment of March 13, 2008 would be entered for the purposes of appeal.

However, The Advisory Action dated August 11, 2008 indicates that the Amendment of March 13, 2008 would ***not*** be entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The Final Office Action at page 2 indicates that claim 9, lines 9-10 will be interpreted as follows:

> *forming base and emitter electrode lead openings within said insulating film, said base electrode lead opening being formed simultaneous with said emitter electrode lead opening.*

Accordingly, the following description is provided for illustrative purposes and is not intended to limit the scope of the invention.

Claim 9 is drawn to a method for manufacturing a bipolar transistor, the method comprising the steps of:	
forming a base layer (18) on an insulator, said base layer (18) being in contact with a portion of a semiconductor substrate;	Specification at page 11, line 25 to page 12, line 13.
forming an insulating film (2) on said base layer (18);	Specification at page 12, lines 15-20.
forming base and emitter electrode lead openings (4, 5) within said insulating film (2), said base electrode lead opening (5) being formed simultaneous with said emitter electrode lead opening (4);	Specification at page 12, lines 22-26.
depositing a conducting film (6) into said base electrode lead opening (5) and into said emitter electrode lead opening (4), said conducting film (6) within said base electrode lead opening (5) being a base electrode lead portion (50) and said conducting film (6) within said emitter electrode lead opening (4) being an emitter electrode lead portion (40); thereafter,	Specification at page 12, line 28 to page 13, line 1.
polishing said conducting film (40, 50) to separate said base electrode lead portion (50) from said emitter electrode lead portion (40).	Specification at page 13, lines 4-7.

Claim 14 is drawn to the method for manufacturing a bipolar transistor as described in claim 9, further comprising the step of depositing a silicide (7) onto a polished surface of said conducting film (40, 50).	Specification at page 13, line 3 to page 14, line 17.

Claim 15 is drawn to the method for manufacturing a bipolar transistor as described in claim 14, further comprising the step of depositing an interlayer insulator (30) onto said silicide (7) and said insulating film (2).	Specification at page 14, line 19 to page 15, line 5.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The issues presented for consideration in this appeal are as follows:

Whether the Examiner erred in rejecting claims 9-13 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 6,307,227 (Fujii) in view of U.S. Patent No. 5,013,677 (Hozumi), and further in view of U.S. Patent No. 6,885,081 (Morimoto).

Whether the Examiner erred in rejecting claims 14-15 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 6,307,227 (Fujii) in view of U.S. Patent No. 5,013,677 (Hozumi), and further in view of U.S. Patent No. 6,885,081 (Morimoto), and further in view of U.S. Patent Application Publication No. 2003/0235984 (Besser).

These issues will be discussed hereinbelow.

VII. ARGUMENT

The Examiner erred in rejecting claims 9-13 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 6,307,227 (Fujii) in view of U.S. Patent No. 5,013,677 (Hozumi), and further in view of U.S. Patent No. 6,885,081 (Morimoto).

This rejection is traversed at least for the following reasons.

Claims 9-13 stand or fall together - Claim 9 includes the step of polishing said conducting film to separate said base electrode lead portion from said emitter electrode lead portion.

The specification as originally filed at page 13, lines 4-7 provide that *next, the polycrystalline silicon is polished using a CMP (chemical mechanical polishing) process until an emitter electrode lead portion 40 and a base electrode lead portion 50 are separated from each other to achieve insulation.*

Figures 5 and 6 of the specification as originally filed are provided hereinbelow.

FIG. 5

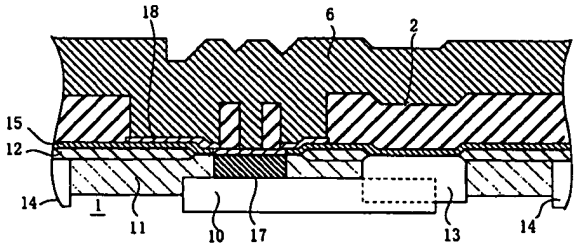
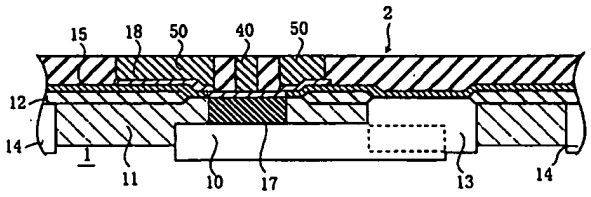


FIG. 6



Fujii - Fujii arguably discloses the presence of a base electrode 13 and an emitter electrode 15 (Fujii at column 4, lines 37 and 39).

Fujii, at column 8, lines 27-30, provides that after this, as shown in FIG. 9, a *first interlayer insulating film 16* is formed over the entire surface, and *holes are made at required positions* and *filled up with polysilicon*, and thereby *first layer contacts 17* are formed.

However, the Office Action readily admits that Fujii fails to teach the holes being simultaneously formed (Office Action at page 4).

- ***Thus, Fujii fails to disclose, teach, or suggest forming base and emitter electrode lead openings within said insulating film, said base electrode lead opening being formed simultaneous with said emitter electrode lead opening.***

The Office Action readily admits that Fujii ***fails*** to teach the step of polishing said conducting film to separate said base electrode lead portion from said emitter electrode lead portion (Final Office Action at page 4).

Hozumi - The Office Action readily admits that Hozumi ***fails*** to teach the step of polishing said conducting film to separate said base electrode lead portion from said emitter electrode lead portion (Final Office Action at page 4).

Morimoto - Morimoto arguably discloses that then, *surface polishing by the CMP method* is performed starting with the surface of the tungsten film 14 to *remove the tungsten and titanium nitride films* other than the film portions filled in the via holes, whereby a plug 14 (same reference number as that for the tungsten film is used for the sake of convenience) made of the titanium nitride film and the tungsten film 14 is formed in each via hole 13, as shown in FIG. 2C (Morimoto at column 6, lines 18-24).

Figures 2B-2C of Morimoto are provided hereinbelow.

Fig. 2B

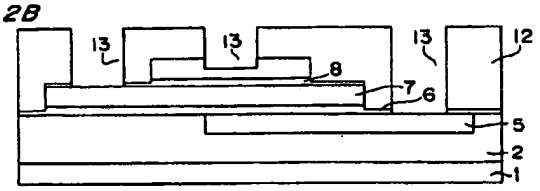
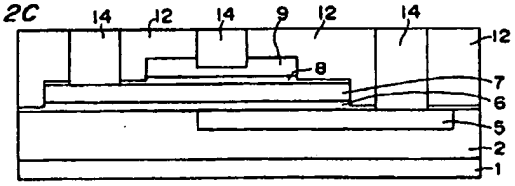


Fig. 2C



However, Morimoto ***fails*** to teach surface polishing by the CMP method to separate one portion 14 from another portion 14.

Even still, Morimoto ***fails*** to teach the presence of a bipolar transistor. Instead, the figures of Morimoto depict a capacitor. That is, as shown in FIG. 3, the first ***MIM capacitor C1*** consists of the lower electrode 5, the first capacitor dielectric film 6 and the upper electrode 7, while the ***second MIM capacitor*** consists of the lower electrode 7, the second capacitor dielectric film 8 and the upper electrode 9 (Morimoto at column 6, lines 37-41).

- ***Thus, Fujii, Hozumi, and Morimoto, either individually or as a whole, fail to disclose, teach or suggest the step of polishing said conducting film to separate said base electrode lead portion from said emitter electrode lead portion.***

The Examiner erred in rejecting claims 14-15 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 6,307,227 (Fujii) in view of U.S. Patent No. 5,013,677 (Hozumi), and further in view of U.S. Patent No. 6,885,081 (Morimoto), and further in view of U.S. Patent Application Publication No. 2003/0235984 (Besser).

In addition to the reasons set forth hereinabove with respect to claims 9-13, this rejection is traversed at least for the following reasons.

Claim 14 stands or falls alone - Claim 14 is drawn to a method for manufacturing a bipolar transistor that includes the step of depositing a silicide (7) onto a polished surface of said conducting film (40, 50).

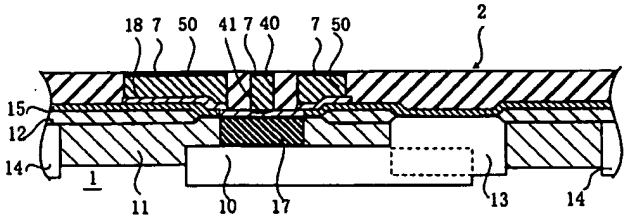
The specification as originally filed at page 13, lines 4-7 provide that *next, the polycrystalline silicon is polished using a* ***CMP (chemical mechanical polishing) process*** *until an emitter electrode lead portion 40 and a base electrode lead portion 50 are separated from each other to achieve insulation.*

Next, a ***metal film*** *of about 15 nm comprised of Co or Ti and a metal film oxidation preventing film of about 30 nm comprised of TiN are successively formed by a sputtering process* (specification as originally filed at page 14, lines 6-8).

The metal film is then subjected to heat treatment by an RTP (rapid thermal process) in, e.g., a nitrogen gas atmosphere at 500.degree. C. for about 30 seconds to form ***metal silicide 7*** (specification as originally filed at page 14, lines 9-11).

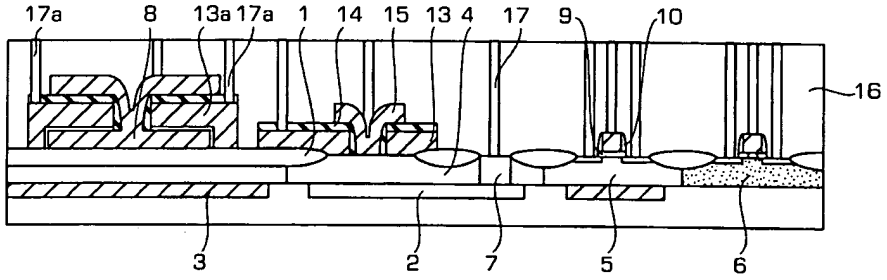
Figure 7 of the specification as originally filed is provided hereinbelow.

FIG. 7



Fujii - Figure 9 of Fujii is provided hereinbelow.

FIG. 9



Fujii arguably discloses that *holes are made at required positions* and *filled up with polysilicon* (Fujii at 8, lines 28-29).

Nevertheless, the Office Action ***readily admits*** that Fujii ***fails*** to disclose, teach or suggest *polishing* the polysilicon to separate the contacts 17 (Final Office Action at page 5).

- ***Thus, Fujii fails to disclose, teach, or suggest polishing said conducting film to separate said base electrode lead portion from said emitter electrode lead portion.***

Fujii arguably discloses that the use of polycide that is ***silicided*** polysilicon with titanium, cobalt, molybdenum, tungsten or the like, is preferable, since it reduces the resistance value of the capacitor further down (Fujii at column 9, lines 55-56).

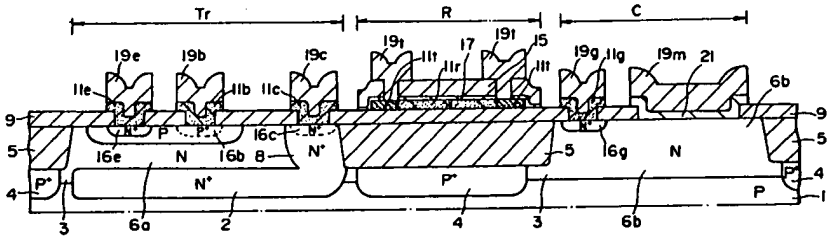
However, Fujii ***fails*** to teach a silicided base electrode lead portion or a silicided emitter electrode lead portion.

Instead, in the first and the second embodiments described above, the first electrode of the ***capacitor*** and the ***gate electrodes*** of the MOSFETs are formed of polysilicon (Fujii at column 9, lines 51-53).

- ***Thus, Fujii fails to disclose, teach, or suggest depositing a silicide onto a polished surface of said conducting film.***

Hozumi - Figure 2M of Hozumi is provided hereinbelow.

FIG. 2M



Hozumi arguably discloses the presence of a base region 7.

However, the Office Action fails to show wherein there is to be found within Hozumi a step of forming the base region 7 on an insulator.

- ***Thus, the Office Action fails to show within Hozumi a step of forming a base layer on an insulator, said base layer being in contact with a portion of a semiconductor substrate.***

- ***Moreover, the Office Action fails to show that Hozumi teaches polishing said conducting film to separate said base electrode lead portion from said emitter electrode lead portion.***

In addition, the Office Action ***fails*** to show wherein there is to be found within Hozumi a silicided base electrode lead portion or a silicided emitter electrode lead portion.

- ***Thus, the Office Action fails to show that Hozumi teaches depositing a silicide onto a polished surface of said conducting film.***

Morimoto - Morimoto arguably discloses that then, *surface polishing by the CMP method* is performed starting with the surface of the tungsten film 14 to *remove the tungsten and titanium nitride films* other than the film portions filled in the via holes, whereby a plug 14 (same reference number as that for the tungsten film is used for the sake of convenience) made of the titanium nitride film and the tungsten film 14 is formed in each via hole 13, as shown in FIG. 2C (Morimoto at column 6, lines 18-24).

Figures 2B-2C of Morimoto are provided hereinbelow.

Fig. 2B

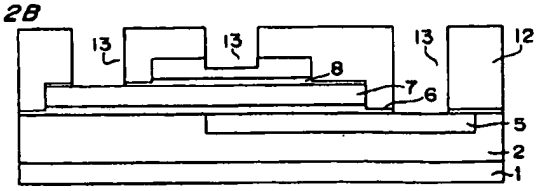
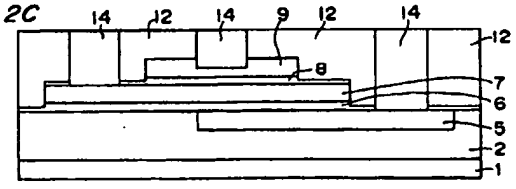


Fig. 2C



Whereas the figures of Morimoto depict a capacitor, Morimoto ***fails*** to teach the presence of a bipolar transistor. Additionally, Morimoto arguably discloses a tungsten plug 14 (Morimoto at column 6, line 19).

However, Morimoto ***fails*** to teach a *silicided* plug 14.

- ***Thus, Morimoto fails to disclose, teach, or suggest depositing a silicide onto a polished surface of said conducting film.***

Besser - Figure 1 of Besser is provided hereinbelow.

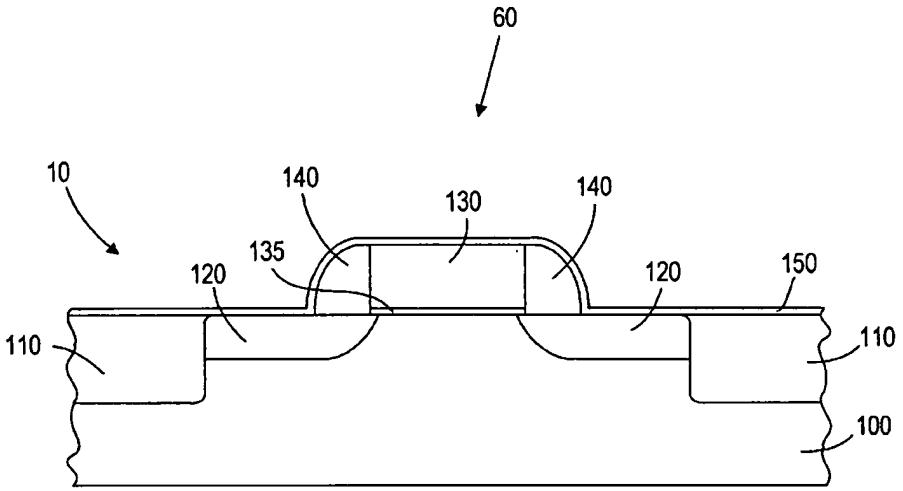


Fig. 1

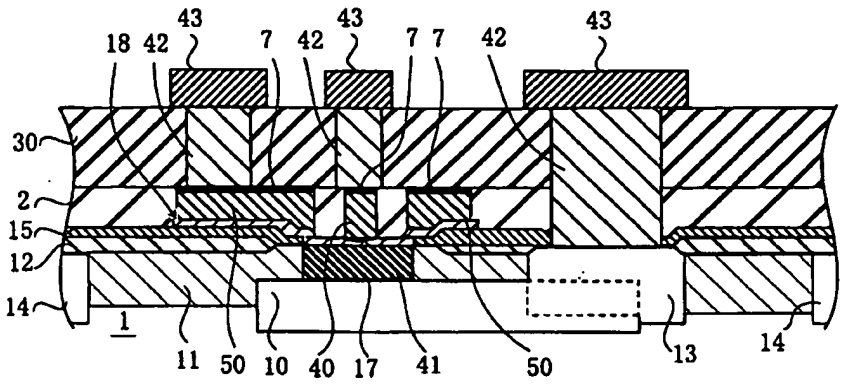
Besser ***fails*** to disclose, teach, or suggest gate region 130 as being polished.

- ***Thus, Besser fails to disclose, teach, or suggest depositing a silicide onto a polished surface of said conducting film.***

Claim 15 stands or falls alone - Claim 15 is drawn to the method for manufacturing a bipolar transistor as described in claim 14, further comprising the step of depositing an interlayer insulator (30) onto said silicide (7) and said insulating film (2).

Figure 8 of the specification is provided hereinbelow.

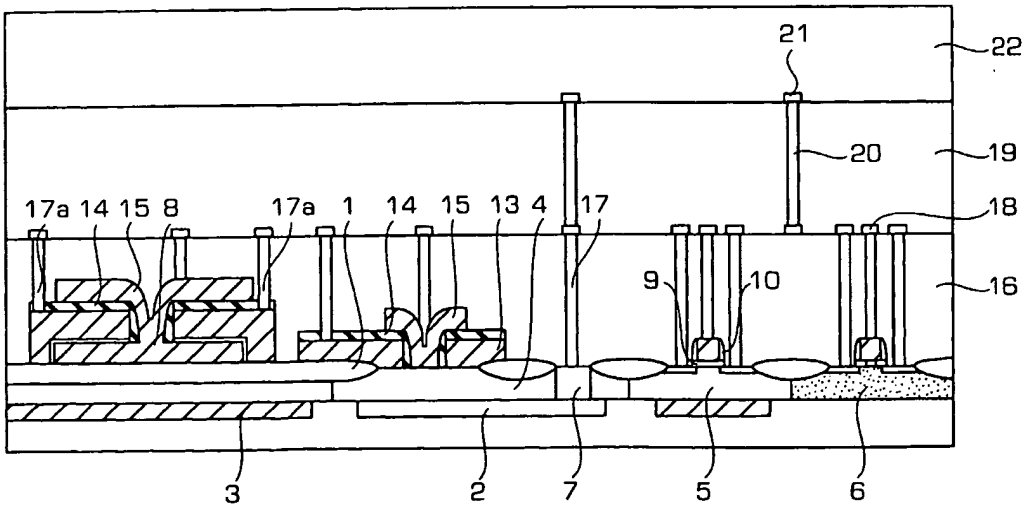
FIG. 8



Fujii - The Office Action contends that Fujii teaches a step of depositing an interlayer insulator 19 onto said silicide and said insulating film (Final Office Action at page 6).

In response, Figure 10 of Fujii is provided hereinbelow for example.

FIG. 10



Next, as shown in FIG. 10, ***a first layer wiring 18 is formed with aluminium or the like*** on the surface of the first interlayer insulating film 16 (Fujii at column 8, lines 39-41).

However, Fujii first layer wiring 18 as being a silicide is ***absent*** from within Fujii.

- ***Thus, Fujii fails to disclose, teach, or suggest the step of depositing an interlayer insulator onto said silicide and said insulating film.***

Hozumi, Morimoto, and Besser - Hozumi, Morimoto, and Besser fail to account for the features that are deficient from within Fujii.

Conclusion

The claims are considered allowable for the same reasons discussed above, as well as for the additional features they recite.

Reversal of the Examiner's decision is respectfully requested.

Dated: September 9, 2008

Respectfully submitted,

By _____

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CLAIMS APPENDIX

1-8. (Canceled)

9. A method for manufacturing a bipolar transistor, the method comprising the steps of:

forming a base layer on an insulator, said base layer being in contact with a portion of a semiconductor substrate;

forming an insulating film on said base layer;

forming base and opening electrode lead openings within said insulating film, said base electrode lead opening being formed simultaneous with said emitter electrode lead opening;

depositing a conducting film into said base electrode lead opening and into said emitter electrode lead opening, said conducting film within said base electrode lead opening being a base electrode lead portion and said conducting film within said emitter electrode lead opening being an emitter electrode lead portion; and thereafter,

polishing said conducting film to separate said base electrode lead portion from said emitter electrode lead portion.

10. The method for manufacturing a bipolar transistor as described in claim 9, wherein said insulator is on said semiconductor substrate, an opening within said insulator exposing said portion of the semiconductor substrate.

11. The method for manufacturing a bipolar transistor as described in claim 9, wherein said base layer is a semiconductor material.

12. The method for manufacturing a bipolar transistor as described in claim 9, wherein said conducting film is deposited simultaneously into said base and emitter electrode lead openings.

13. The method for manufacturing a bipolar transistor as described in claim 9, further comprising the step of:

diffusing a dopant from said emitter electrode lead portion into said base layer to form an emitter region with said base layer.

14. The method for manufacturing a bipolar transistor as described in claim 9, further comprising the step of:

depositing a silicide onto a polished surface of said conducting film.

15. The method for manufacturing a bipolar transistor as described in claim 14, further comprising the step of:

depositing an interlayer insulator onto said silicide and said insulating film.

EVIDENCE APPENDIX

There is no other evidence which will directly affect or have a bearing on the Board's decision in this appeal.

RELATED PROCEEDINGS APPENDIX

There are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.